Docket No.: M4065.0624/P624
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:
Howard E. Rhodes

Application No.: 10/751,439 Confirmation No.: 3917

Filed: January 6, 2004 Art Unit: 2818

For: METHOD AND APPARATUS PROVIDING CMOS IMAGER DEVICE PIXEL WITH TRANSISTOR HAVING LOWER THRESHOLD VOLTAGE THAN OTHER IMAGER DEVICE TRANSISTORS

Examiner: D. Nhu

## APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on September 19, 2006, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

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This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

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|---|---|
| I. | Real Party In Interest |
| II | Related Appeals and Interferences |
| III. | Status of Claims |
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| V. | Summary of Claimed Subject Matter |
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## I. REAL PARTY IN INTEREST

The real party in interest for this appeal is Micron Technology, Inc., the assignee of this application.

## II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

## III. STATUS OF CLAIMS

### A. Total Number of Claims in Application

There are 46 claims pending in application. The application contains claims 1-2, 4-18, 20-41, and 43-49, which were finally rejected. This is an appeal from the final rejection of claims 1-2, 4-18, 20-41, and 43-49.

B. Current Status of Claims

1. Claims canceled: 3, 19, 42, and 50-143.

2. Claims withdrawn from consideration but not canceled: None.

3. Claims pending: 1-2, 4-18, 20-41, and 43-49.

4. Claims allowed: None

5. Claims rejected: 1-2, 4-18, 20-41, and 43-49.

C. Claims On Appeal

The claims on appeal are claims 1-2, 4-18, 20-41, and 43-49.

## IV. STATUS OF AMENDMENTS

Appellant filed an Amendment After Final Action on July 18, 2006. The Examiner responded to the Amendment After Final Action in an Advisory Action mailed August 28, 2006. In the Advisory Action, the Examiner considered the Amendment as a Request for Reconsideration, and indicated that Appellant's arguments were considered, but were not deemed to place the application in condition for allowance. The Examiner also indicated in the Advisory Action that the amendments to claims 1, 4, 7-8, 12-13, 16, 18, 20-21, 25-27, 30-33, 37-40, 43-44, and 47-49 would be entered for the purposes of an appeal. The claims as set forth in Appendix A of this brief contain these amendments.

## V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention is directed to a pixel cell transistor for improving output signal efficiency of a pixel cell. Specification, paragraph [0001].

Conventional pixel cells, such as those disclosed in the reference to Hong (U.S. Patent Application No. 2005/0040393), which is used to reject all of the claims, use halo, enhancement, and lightly doped drain (LDD) implants in source and drain regions of transistors to minimize short-channel effects, reduce degradation in the threshold voltage, and decrease the electric field to an acceptable level near the edges of the gate of the transistors. Specification paragraph [0010]. However, halo, enhancement, and LDD implants provide a relatively high turn-on threshold voltage of typically 0.8 V, which limits the signal output swing or range which can be obtained from the pixel cell. Specification paragraph [0011]. This limits the dynamic range of a light signal which can be output by a pixel.

In the present invention, at least one transistor of the pixel cell may be formed to have a lower threshold voltage than that of other transistors employed in an imaging device containing the pixel cell by eliminating at least one of a halo implant, an enhancement implant and an LDD implant on at least one side of the gate of the transistor. Specification paragraph [0016]. The lower threshold voltage increases the maximum swing voltage for a source follower transistor used in a pixel for providing an output signal and the maximum reset voltage applied to the floating diffusion region by the reset transistor of a pixel. Specification paragraph [0012]. Lower threshold voltages for other pixel transistors may also be desirable. *Id.* The invention also includes methods of fabricating the pixel cell, and processor systems including the pixel cell. Specification paragraphs [0043]-[0072].

Accordingly, independent claim 1 recites a "method of forming a pixel cell of an imaging device, said method comprising the steps of: forming a photosensitive device in said pixel cell; and forming at least one transistor in said pixel cell to have a gate and source/drain regions on opposite sides of said gate, at least one of said source/drain

regions having no halo implant, wherein at least one of said source/drain regions has no lightly doped drain implant." Specification paragraphs [0043]-[0072].

Independent claim 16 recites a "method of forming a pixel cell of an imaging device, said method comprising the steps of: forming a photosensitive device in said pixel cell; and forming at least one transistor in said pixel cell to have a gate receiving charge from said photosensitive device and source/drain regions on opposite sides of said gate, at least one of said source/drain regions having no enhancement implant, wherein at least one of said source/drain regions has no lightly doped drain implant." Specification paragraphs [0043]-[0072].

Independent claim 28 recites a "method of forming a pixel cell of an imaging device, said method comprising the steps of: forming a photosensitive device in said pixel cell; and forming at least one transistor in said pixel cell to have a gate receiving charge from said photosensitive device and source/drain regions on opposite sides of said gate, at least one of said source/drain regions having no lightly doped drain implant." Specification paragraphs [0043]-[0072].

Independent claim 40 recites a "method of forming a pixel cell of an imaging device, said method comprising the steps of: forming a photosensitive device in said pixel cell; forming a first transistor in said pixel cell to have a first gate receiving charge from said photosensitive device and first source/drain regions on opposite sides of said first gate; and forming a second transistor in said pixel cell to have a second gate for resetting a signal from said first transistor and second source/drain regions on opposite sides of said second gate, at least one of said second source/drain regions having no halo implant, wherein at least one of said second source/drain regions has no lightly doped drain implant." Specification paragraphs [0043]-[0072].

## VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1-2, 4-18, 20-41, and 43-49 are properly rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application No. 2005/0040393 to Hong (hereinafter "Hong").

## VII. ARGUMENT

### A. Claims 1-2, 4-18, 20-41, and 43-49 are Not Anticipated by the Disclosure of Hong.

#### 1. The Independent Claims Are Not Anticipated by Hong.

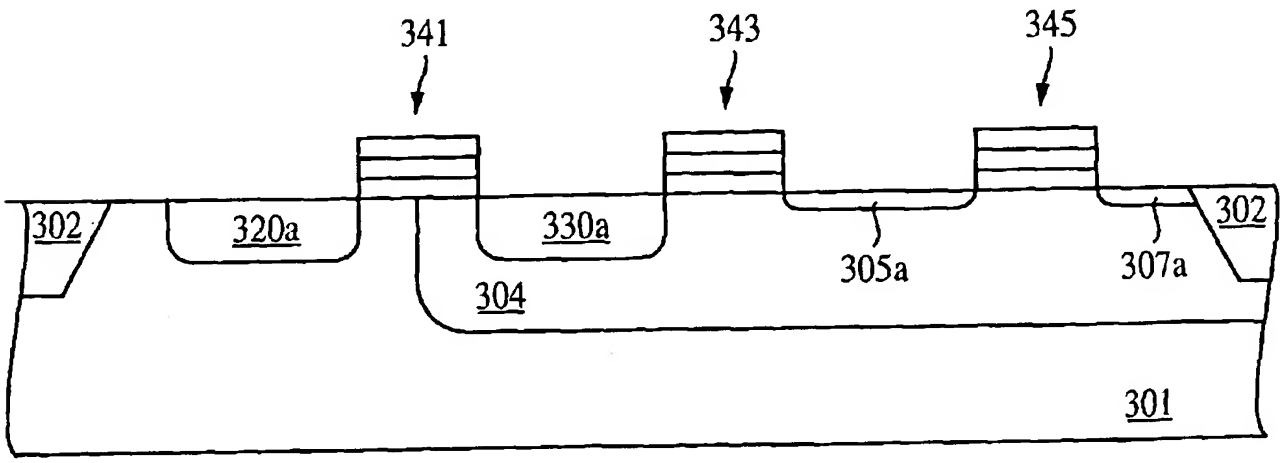
Claim 1 recites a method of forming a pixel cell of an imaging device comprising, *inter alia*, "forming at least one transistor in said pixel cell to have a gate and source/drain regions on opposite sides of said gate, at least one of said source/drain regions having no halo implant" (emphasis added). In addition, per claim 1, "at least one of said source/drain regions has no lightly doped drain implant" (emphasis added). Appellant respectfully submits that Hong does not disclose the above claim limitations.

To the contrary, Hong discloses in the description of FIG. 5F (reproduced below), which is a cross section of the pixel 300, shown in FIGs. 2B and 4A-4C, that "lightly doped drain (LDD) implants are performed by known techniques to provide LDD regions 305a and 307a." Hong paragraph [0054] (emphasis added). LDD regions 305a and 307a are part of the source/drain regions of reset transistor 345. Hong. FIG. 5F. This is consistent with the discussion in the background of the present application, which notes that halo, enhancement, and LDD implants are commonly used on the transistors of conventional pixel cells.

Although the May 19, 2006, Office Action takes the position that FIGs. 4A-4C show no LDD implant (p. 4), these figures are schematic views of the same pixel shown

in cross-section in FIG. 5F, and neither show the detail illustrated in FIG. 5F nor illustrate any implant patterns. *See* Hong paragraphs [0017]-[0019], and [0025]. Hong does not disclose formation of any other source or drain regions for any other transistor, nor is there a disclosure of the omission of a LDD implant with respect to any other transistor. Accordingly, Hong does not disclose "no lightly doped drain implant". Furthermore, Hong also fails to disclose the omission of halo implants, as also recited in claim 1.

Hong FIG. 5F




Therefore, since there is no disclosure of at least one of said source/drain regions having no halo implant, or of at least one of the source/drain regions having no lightly doped drain implant, as recited in claim 1, claim 1 and its dependent claims 2-15 are not anticipated by Hong.

It is settled law that, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). Moreover, "[t]he fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or

characteristic." *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

Hong does not expressly or inherently disclose the absence of a halo implant or the absence of an LDD implant.

Claim 16 recites a method of forming a pixel cell of an imaging device comprising, *inter alia*, "forming at least one transistor in said pixel cell to have a gate receiving charge from said photosensitive device and source/drain regions on opposite sides of said gate, at least one of said source/drain regions having no enhancement implant, wherein at least one of said source/drain regions has no lightly doped drain implant" (emphasis added). Hong does not disclose these limitations.

To the contrary, Hong discloses in the description of FIG. 5F, which is part of the fabrication of the pixel 300, shown in FIGs. 2B and 4A-4C, that "lightly doped drain (LDD) implants are performed by known techniques to provide LDD regions 305a and 307a." Hong paragraph [0054] (emphasis added). LDD regions 305a and 307a are part of source/drain regions of reset transistor 345, which receives a reset signal at its gate; there is no disclosure of the omission of a LDD implant with respect to any other transistor, and particularly for a pixel transistor which receives charge from a photosensitive device at its gate. Hong. FIG. 5F. Furthermore, Hong also fails to disclose the omission of enhancement implants for any transistor, much less for a pixel

transistor which receives charge from a photosensitive device at its gate. Therefore, since Hong does not disclose the omission of a LDD implant and omission of an enhancement implant for a transistor receiving charge from a photosensitive device at its gate, claim 16 and its dependent claims 17-27 are not anticipated by Hong.

Claim 28 recites a method of forming a pixel cell of an imaging device comprising, *inter alia*, "forming at least one transistor in said pixel cell to have a gate receiving charge from said photosensitive device and source/drain regions on opposite sides of said gate, at least one of said source/drain regions having no lightly doped drain implant" (emphasis added). Hong does not disclose this limitation.

To the contrary, and as noted, Hong discloses in the description of FIG. 5F, which is part of the fabrication of the pixel 300, shown in FIGs. 2B and 4A-4C, that "lightly doped drain (LDD) implants are performed by known techniques to provide LDD regions 305a and 307a." Hong paragraph [0054] (emphasis added). LDD regions 305a and 307a are part of source/drain regions of reset transistor 345, which receives a reset signal at its gate. Hong. FIG. 5F. Appellant respectfully submits that Hong does not disclose a transistor having a gate receiving charge from a photosensitive device, at least one of the source/drain regions of which has no lightly doped drain implant, as recited in claim 28. Accordingly, claim 28 and its dependent claims 29-39 are not anticipated by Hong.

Claim 40 recites a method of forming a pixel cell of an imaging device comprising, *inter alia*, "forming a first transistor in said pixel cell to have a first gate receiving charge from said photosensitive device and first source/drain regions on opposite sides of said first gate; and forming a second transistor in said pixel cell to have a second gate for resetting a signal from said first transistor and second source/drain regions on opposite sides of said second gate, at least one of said second

source/drain regions having no halo implant, wherein at least one of said source/drain regions has no lightly doped drain implant" (emphasis added). Hong does not disclose these limitations.

To the contrary, and as again noted, Hong discloses in the description of FIG. 5F, which is part of the fabrication of the pixel 300, shown in FIGs. 2B and 4A-4C, that "lightly doped drain (LDD) implants are performed by known techniques to provide LDD regions 305a and 307a." Hong paragraph [0054] (emphasis added). LDD regions 305a and 307a are part of source/drain regions of reset transistor 345. Hong. FIG. 5F. Furthermore, Hong does not disclose the omission of halo implants. Therefore, since Hong does not show the omission of halo implants from at least one of the source/drain regions of the reset transistor, or the omission of LDD implants from the source/drain regions of either (a) a transistor receiving charge from a photosensitive device at its gate, or (b) a reset transistor, claim 40 and its dependent claims 41-49 are not anticipated by Hong.

Since Hong does not disclose all the limitations of claims 1, 16, 28, and 40, claims 1, 16, 28, and 40 are not anticipated by Hong. Claims 2, 4-15, 17-18, 20-27, 29-41, and 43-49 depend, respectively, from claims 1, 16, 28, and 40, and are patentable at least for the reasons mentioned above, and on their own merits. Appellant respectfully requests that the 35 U.S.C. § 102(e) rejection of claims 1-2, 4-18, 20-41, and 43-49 be reversed.

2. The Dependent Claims Are Also Not Anticipated by Hong.

Claims 2, 18, 30, and 41 recite the additional limitation "wherein said source/drain regions on either side of said gate have no halo implant," in addition to the limitations of independent claims 1, 16, 28, and 40, respectively. Hong is silent with respect to halo implants. Therefore, it does not disclose omission of a halo implant on either side of the transistor gate, and this cannot anticipate claims 2, 18, 30, and 41.

Claim 29 recites the limitation "wherein said source/drain regions on either side of said gate have no lightly doped drain implant," in addition to the limitations of independent claims 1, 16, 28, and 40, respectively. As discussed above, Hong discloses in the description of FIG. 5F, which is part of the fabrication of the pixel 300, shown in FIGs. 2B and 4A-4C, that "lightly doped drain (LDD) implants are performed by known techniques to provide LDD regions 305a and 307a." Hong paragraph [0054] (emphasis added). Therefore, Appellant respectfully submits that Hong does not disclose, teach, or suggest all the limitations of claim 29.

Claims 4, 17, and 43 recite the limitation "wherein at least one of said source/drain regions has no enhancement implant," in addition to the limitations of claims 1, 16, and 40, respectively. Claim 5 recites the limitation "wherein both of said source/drain regions have no enhancement implant," in addition to the limitations of independent claim 1. Hong does not disclose the omission of enhancement implants. Therefore, Appellant respectfully submits that Hong does not disclose, teach, or suggest all the limitations of claims 4, 17, and 43.

Claims 7, 12, 20, 25, 32, and 47 recite the limitation "wherein said transistor is selected from the group consisting of: a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer transistor, and a global shutter transistor," in addition to the limitations of independent claims 1, 16, 28, and 40, respectively. Hong discloses only LDD regions 305a and 307a on both sides of a reset transistor 345. Hong does not disclose the omission of LDD regions for at least one of "a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer transistor, and a global shutter transistor." Therefore, Appellant respectfully submits that Hong does not disclose, teach, or suggest all the limitations of claims 7, 12, 20, 25, 32, and 47.

Claims 10-11, 22, 24, 35-36, and 46 recite the limitation "wherein said threshold voltage of said transistor is in the range of about 0.3 V to about less than 0.7 V," in addition to the limitations of independent claims 1, 16, 28, and 40, respectively. The May 19, 2006 Office Action admits (p. 6) that Hong does not disclose this limitation. The Office Action cites paragraphs [0011]-[0020] of the present application to cure Hong's deficiency.

The range of 0.3 V to 0.7 V is disclosed only in the Summary section of the present application (paragraph [0016]), which is not prior art to the claimed invention, and is therefore improperly cited by the Office Action (p. 6). The only value for a threshold voltage disclosed in the Background section is 0.8 V, which is not within the claimed range, and which is obtained with halo, enhancement, and LDD implants. Accordingly, Appellant respectfully submits that Hong does not disclose, teach, or suggest all the limitations of claims 10-11, 22, 24, 35-36, and 46.

For at least these reasons, Appellant respectfully submits that claims 1-2, 4-18, 20-41, and 43-49 are not anticipated by Hong. Accordingly, reversal of the final rejection of these claims is respectfully requested.

## VIII. CONCLUSION

For each of the foregoing reasons, Appellant respectfully submits that the claimed invention is novel over the cited prior art. Reversal of the final grounds of rejection is respectfully solicited.

Dated: November 20, 2006

Respectfully submitted,

By_____

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## APPENDIX A – CLAIMS APPENDIX

**Claims Involved in the Appeal of Application Serial No.** 10/751,439

1. (Previously Presented) A method of forming a pixel cell of an imaging device, said method comprising the steps of:

forming a photosensitive device in said pixel cell; and

forming at least one transistor in said pixel cell to have a gate and source/drain regions on opposite sides of said gate, at least one of said source/drain regions having no halo implant,

wherein at least one of said source/drain regions has no lightly doped drain implant.

2. (Original) The method of claim 1, wherein said source/drain regions on either side of said gate have no halo implant.

3. (Canceled)

4. (Previously Presented) The method of claim 1, wherein at least one of said source/drain regions has no enhancement implant.

5. (Original) The method of claim 4, wherein both of said source/drain regions have no enhancement implant.

6. (Original) The method of claim 1, wherein at least one of said source/drain regions consists essentially of a source/drain implant and a lightly doped drain implant.

7. (Previously Presented) The method of claim 1, wherein said transistor is selected from the group consisting of: a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer transistor, and a global shutter transistor.

8. (Previously Presented) The method of claim 1, wherein said pixel cell is selected from the group consisting of a 3T, 4T, 5T, 6T, and 7T pixel cell.

9. (Original) The method of claim 1, wherein said transistor has a threshold voltage lower than the threshold voltage of another transistor of said pixel cell.

10. (Original) The method of claim 9, wherein said threshold voltage of said transistor is in the range of about 0.3 V to about less than 0.7 V.

11. (Original) The method of claim 10, wherein said threshold voltage of said transistor is about 0.4 V to about 0.65 V.

12. (Previously Presented) The method of claim 9, wherein said another transistor is selected from the group consisting of: a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer gate transistor, and a global shutter transistor.

13. (Previously Presented) The method of claim 1, wherein said photosensitive device is selected from the group consisting of: a photodiode, a photoconductor, and a photogate.

14. (Original) The method of claim 1, wherein said imaging device is a CMOS imager.

15. (Original) The method of claim 1, wherein said imaging device is a CCD imager.

16. (Previously Presented) A method of forming a pixel cell of an imaging device, said method comprising the steps of:

forming a photosensitive device in said pixel cell; and

forming at least one transistor in said pixel cell to have a gate receiving charge from said photosensitive device and source/drain regions on opposite sides of said gate, at least one of said source/drain regions having no enhancement implant,

wherein at least one of said source/drain regions has no lightly doped drain implant.

17. (Original) The method of claim 16, wherein both of said source/drain regions have no enhancement implant.

18. (Previously Presented) The method of claim 16, wherein at least one of said source/drain regions has no halo implant.

19. (Canceled)

20. (Previously Presented) The method of claim 16, wherein said transistor is selected from the group consisting of: a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer gate transistor, and a global shutter transistor.

21. (Previously Presented) The method of claim 16, wherein said pixel cell is selected from the group consisting of: a 3T, 4T, 5T, 6T, and 7T pixel cell.

22. (Original) The method of claim 16, wherein said transistor has a threshold voltage lower than the threshold voltage of another transistor of said pixel cell.

23. (Original) The method of claim 22, wherein said threshold voltage of said transistor is in the range of about 0.3 V to about less than 0.7 V.

24. (Original) The method of claim 23, wherein said threshold voltage of said transistor is about 0.4 V to about 0.65 V.

25. (Previously Presented) The method of claim 22, wherein said another transistor is selected from the group consisting of: a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer gate transistor, and a global shutter transistor.

26. (Previously Presented) The method of claim 16, wherein said photosensitive device is selected from the group consisting of: a photodiode, a photoconductor, and a photogate.

27. (Previously Presented) The method of claim 16, wherein said imaging device is selected from the group consisting of: a CMOS imager or a CCD imager.

28. (Original) A method of forming a pixel cell of an imaging device, said method comprising the steps of:

forming a photosensitive device in said pixel cell; and

forming at least one transistor in said pixel cell to have a gate receiving charge from said photosensitive device and source/drain regions on opposite sides of said gate, at least one of said source/drain regions having no lightly doped drain implant.

29. (Original) The method of claim 28, wherein said source/drain regions on either side of said gate have no lightly doped drain implant.

30. (Previously Presented) The method of claim 28, wherein at least one of said source/drain regions has no halo implant.

31. (Previously Presented) The method of claim 28, wherein at least one of said source/drain regions consists essentially of a source/drain implant and a lightly doped drain implant.

32. (Previously Presented) The method of claim 28, wherein said transistor is selected from the group consisting of: a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer transistor, and a global shutter transistor.

33. (Previously Presented) The method of claim 28, wherein said pixel cell is selected from the group consisting of a 3T, 4T, 5T, 6T, or 7T pixel cell.

34. (Original) The method of claim 28, wherein said transistor has a threshold voltage lower than the threshold voltage of another transistor of said pixel cell.

35. (Original) The method of claim 34, wherein said threshold voltage of said transistor is in the range of about 0.3 V to about less than 0.7 V.

36. (Original) The method of claim 35, wherein said threshold voltage of said transistor is about 0.4 V to about 0.65 V.

37. (Previously Presented) The method of claim 34, wherein said another transistor is selected from the group consisting of: a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer gate transistor, and a global shutter transistor.

38. (Previously Presented) The method of claim 28, wherein said photosensitive device is selected from the group consisting of: a photodiode, a photoconductor, and a photogate.

39. (Previously Presented) The method of claim 28, wherein said imaging device is selected from the group consisting of: a CMOS imager or a CCD imager.

40. (Previously Presented) A method of forming a pixel cell of an imaging device, said method comprising the steps of:

forming a photosensitive device in said pixel cell;

forming a first transistor in said pixel cell to have a first gate receiving charge from said photosensitive device and first source/drain regions on opposite sides of said first gate; and

forming a second transistor in said pixel cell to have a second gate for resetting a signal from said first transistor and second source/drain regions on

opposite sides of said second gate, at least one of said second source/drain regions having no halo implant,

wherein at least one of said second source/drain regions has no lightly doped drain implant.

41. (Original) The method of claim 40, wherein said second source/drain regions on either side of said second gate have no halo implant.

42. (Canceled)

43. (Previously Presented) The method of claim 40, wherein at least one of said second source/drain regions has no enhancement implant.

44. (Previously Presented) The method of claim 40, wherein said pixel cell is selected from the group consisting of: a 3T, 4T, 5T, 6T, and 7T pixel cell.

45. (Original) The method of claim 40, wherein said second transistor has a threshold voltage lower than the threshold voltage of said first transistor of said pixel cell.

46. (Original) The method of claim 44, wherein said threshold voltage of said second transistor is in the range of about 0.3 V to about less than 0.7 V.

47. (Previously Presented) The method of claim 40, wherein said first transistor and said second transistor are independently selected from the group consisting of: a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer gate transistor, and a global shutter transistor.

48. (Previously Presented) The method of claim 40, wherein said photosensitive device is selected from the group consisting of a photodiode, a photoconductor and, a photogate.

49. (Previously Presented) The method of claim 40, wherein said imaging device is selected from the group consisting of: a CMOS imager or a CCD imager.

50-143. (Canceled)

## APPENDIX B – EVIDENCE APPENDIX

NONE

## APPENDIX C – RELATED PROCEEDINGS APPENDIX

NONE

# TRANSMITTAL OF APPEAL BRIEF

Docket No.
M4065.0624/P624

In re Application of: Howard E. Rhodes

| Application No. | Filing Date | Examiner | Group Art Unit |
|---|---|---|---|
| 10/751,439-Conf. #3917 | January 6, 2004 | D. Nhu | 2818 |

Invention: METHOD AND APPARATUS PROVIDING CMOS IMAGER DEVICE PIXEL WITH TRANSISTOR HAVING LOWER THRESHOLD VOLTAGE THAN OTHER IMAGER DEVICE TRANSISTORS

**TO THE COMMISSIONER OF PATENTS:**

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: September 19, 2006 .

The fee for filing this Appeal Brief is $ 500.00 .

[x] Large Entity [ ] Small Entity

[ ] A petition for extension of time is also enclosed.

The fee for the extension of time is _____ .

[ ] A check in the amount of _____ is enclosed.

[ ] Charge the amount of the fee to Deposit Account No. 04-1073 .
This sheet is submitted in duplicate.

[x] Payment by credit card. Form PTO-2038 is attached.

[x] The Director is hereby authorized to charge any additional fees that may be required or credit any overpayment to Deposit Account No. 04-1073 .
This sheet is submitted in duplicate.

Dated: November 19, 2006

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